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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,120	09/22/2003	Takashi Miyazawa	117244	5416

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/665,120	MIYAZAWA, TAKASHI	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,13,14 and 20-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,13,14 and 20-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 19 January 2007 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1-8, 13-14 and 20-31 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 6-8, 13-14, 20, 22-24 and 28-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Howard (US 2003/0052614).

Regarding claim 1, Howard discloses an electronic circuit (Figure 3A), comprising:

a capacitor stores a current signal supplied to the capacitor during a first period and a voltage signal supplied to the capacitor during a second period (Figure 3A capacitor C1, where paragraph [0028] explains that during a first period the capacitor is charged using the input data current level and paragraph [0029] explains that during a second period the capacitor is charged to a level corresponding of the reverse bias, i.e. voltage level shown in Figure 3A.); and

a first transistor that includes a first gate, a first drain and a first source (Figure 3A shows transistor Q1 which has a gate 321, a source 323 and a drain 325.),

a conduction state of the first transistor being set in accordance with a charge stored by the capacitor (Paragraphs [0028]-[0029] explain the state of the capacitor C1 determined whether Q1 is on or off.),

a first current as the current signal flowing through the first transistor during at least a part of the first period (Paragraph [0028] explains that current level according to the input data current level flows through the transistor during a first period.), and

no current flowing through the first transistor during at least a part of the second period (Paragraph [0029] explains that during a part of the second period the TFT current driver Q1 is biased off, which means that no current will be flowing through the transistor.).

Regarding claim 2, Howard discloses the electronic circuit according to Claim 1, further comprising:

a second transistor (Figure 3A, Q3),

the current signal and the voltage signal being supplied to the capacitor through the second transistor (I_{data} and V_{rev} must be supplied to the capacitor C1 through Q3.).

Regarding claim 3, Howard discloses the electronic circuit according to Claim 1, further comprising:

a third transistor (Figure 3A, Q4) that controls an electronic connection between the first gate and the first drain (As shown in Figure 3A the transistor Q4 has its drain connected to the gate of Q1 meaning that Q4 will control Q1's electrical connection.).

Regarding claim 6, Howard an electro-optical device, comprising:

a plurality of scanning lines (Figure 1, Row Select line 106);

a plurality of data lines (Figure 1, Column Select (Data) item 104);

a plurality of electro-optical elements that are disposed corresponding to intersections between the plurality of scanning lines and the plurality of data lines (Figure 1 shows electro-optical elements 110):

a first electrode that is disposed opposite to a plurality of second electrodes, each of which is included in one electro-optical element of the plurality of electro-optical elements (As shown in Figure 1, each electro-optical element 110 has a second electrode connected to each respective transistor 108, while the other electrode of all of them is commonly connected to ground.);

a first circuit that outputs a current signal that is accumulated in a capacitor included in each of the plurality of unit circuits (Figure 3A shows current signal I_{data}, which would come from a first circuit for input to the data line so as to charge the capacitor as stated in paragraph [0028].), each of which includes one electro- optical element of the plurality of electro-optical elements (Figure 1 shows that each unit circuit has an electro-optical element.); and

a second circuit that outputs a voltage signal that is accumulated in a capacitor in each of the plurality of unit circuits (Figure 3A shows voltage signal V_{rev}, which would come from a second circuit for input to the data line so as to charge the capacitor as stated in paragraph [0029].).

Regarding claim 7, Howard discloses the electro-optical device according to Claim 6,

the current signal and voltage signal being supplied to each of the plurality of unit circuits through one data line of the plurality of data lines (Figure 3A shows line 308.).

Regarding claim 8, Howard discloses the electro-optical device according to Claim 6,

the plurality of data lines including a plurality of first data lines and a plurality of second data lines (Figure 3A shows 339 and 337),

the current signal being supplied to each of the plurality of unit circuits through one first data line of the plurality of first data lines (Figure 3A shows the current signal being supplied through 339.); and

the voltage signal being supplied to each of the plurality of unit circuits through one second data line of the plurality of second data lines (Figure 3A shows the voltage signal being supplied through 337.).

Regarding claim 13, Howard discloses the electro-optical device according to Claim 22, the electro-optical element being an EL element (Figure 3A, OLED 306).

Regarding claim 14, Howard discloses the electro-optical device according to Claim 13, the EL element including a light-emitting layer that is composed of an organic material (Figure 3A, the O in OLED stands for organic.).

Regarding claim 20, Howard discloses an electronic apparatus, comprising: the electro-optical device according to Claim 6 (Figure 1 and paragraph [0001]).

Regarding claim 22, Howard discloses the electro-optical device according to Claim 6, each of the plurality of unit circuits including an electro-optical element (Figure 1 shows that each unit circuit has an OLED.).

Regarding claim 23, Howard discloses an electronic circuit, comprising:

a capacitor that accumulates a current signal that is received by the electronic circuit during a first period (Figure 3A capacitor C1, where paragraph [0028] explains that during a first period the capacitor is charged using the input data current level.), the capacitor accumulating a voltage signal that is received by the electronic circuit during a second period (Paragraph [0029] explains that during a second period the capacitor is charged to a level corresponding of the reverse bias, i.e. voltage level shown in Figure 3A.); and

a first transistor whose conduction state is set in accordance with an amount of charge accumulated in the capacitor stored during a selected period from the first period and the second period (Paragraphs [0028]-[0029] explain that the transistor is on or off dependent on the charge stored in capacitor C1.),

the first transistor including a first gate, a first drain and a first source (Figure 3A shows transistor Q1 which has a gate 321, a source 323 and a drain 325.), the first transistor supplying a current whose amount is determined in accordance with the

conduction state to an electronic element (Figure 3A shows that based on the transistor Q1 being on or off will determine whether current is supplied to the OLED.).

Regarding claim 24, please refer to the rejection of claim 23, where the first mode is a current mode corresponding to the first period, and the second mode is a voltage mode that corresponds to the second period.

Regarding claim 28, this claim is rejected under the same rationale as claim 2.

Regarding claim 29, this claim is rejected under the same rationale as claim 3.

Regarding claim 30, Howard disclose the electronic circuit according to claim 1, further comprising:

an electronic element (Figure 3A, OLED),

a second current whose current level corresponds to the conduction state of the first transistor being supplied to the electronic element (Paragraph [0028], last sentence).

Regarding claim 31, Howard disclose the electronic circuit according to claim 6,

a potential of the first electrode being set at a constant during at least a part of a first period in which the current signal is supplied to the capacitor (Figure 3A shows that the first electrode is always connected to ground, which is a constant.), and

the potential of the first electrode being set at the constant during at least a part of a second period in which the voltage signal is supplied to the capacitor (Figure 3A shows that the first electrode is always connected to ground, which is a constant.).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Howard (US 2003/0052614) in view of Dawson (US 6,229,506).

Regarding claim 4, Howard discloses the electronic circuit according to Claim 1.

Howard fails to teach a fourth transistor that controls a timing to start or stop supply of the current to the electronic element after the conduction state of the first transistor is set according to at least one of the current signal and the voltage signal.

Dawson discloses a fourth transistor (Figure 2, element 250; column 3, lines 36-39 and lines 55-57) that controls a timing to start or stop supply of current to an electronic element after the conduction state of a first transistor (Figure 2, item 260) is set according to at least one of a current signal and a voltage signal.

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to include a transistor as taught by Dawson into the pixel circuit taught by Howard in order to provide for a way to provide stabilization to the TFTs in the pixel circuit.

Regarding claim 5, the electronic circuit according to Claim 1.

Howard fails to teach a fifth transistor, the amount of charge held in the capacitor being reset to a predetermined state when the fifth transistor is turned on.

Dawson discloses a transistor, the amount of charge held in a capacitor being reset to a predetermined state when the transistor is turned on (Figure 2, item 270; column 3, lines 20-22 and lines 44-52).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to include a reset transistor as taught by Dawson into the pixel circuit taught by Howard in order to reduce current nonuniformities and threshold voltage variations in a drive transistor.

8. Claims 21 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Howard (US 2003/0052614) in view of Adachi et al. (US 2003/0058195).

Regarding claim 21, Howard discloses the electronic circuit according to Claim 1.

Howard discloses of the voltage signal being a binary data voltage (Figure 3A and paragraphs [0028]-[0029] explain that the voltage is either supplied, i.e. zero voltage or is V_{rev} which is a certain voltage, meaning that the voltage signal is a binary data voltage since it only goes between zero and a value.).

Howard fails to teach the current signal being a multi-valued data current.

Adachi teaches a data current being a multi-value data current (Paragraph [0033], lines 2-8; and paragraph [0097]).

Therefore, it would have been obvious for a person of ordinary skill in the art at the time the invention was made to use data current being a multi-value data current, as taught by Adachi, to the electronic circuit of Howard, so as to be able to increase the number of display gray scale without increasing the number of subframes (Paragraph [0033], lines 6-8) and to prevent image quality degradation such as dynamic contouring without increasing power (Paragraph [0104]).

Regarding claim 25, this claim is rejected under the same rationale as claim 21.

Regarding claim 26, this claim is rejected under the same rationale as claim 21.

9. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Howard (US 2003/0052614) in view of Senda et al. (Pub. No.: US 2002/0171607 A1).

Regarding claim 27, Howard discloses the electronic circuit according to Claim 24.

Howard fails to teach of power consumption in the second mode being lower than a power consumption in the first mode.

Senda teaches switching between an analog image signal display, which is a first mode and a digital image signal display, which is a second mode. Senda teaches the second mode is lower in power consumption than in the first mode (Paragraph [0019], lines 1-6).

It would have been obvious for a person of ordinary skill in the art to have a power consumption in the second mode being lower than a power consumption in the first mode, as taught by Senda to the electronic circuit of Howard, so a to provide a device with power saving capabilities (Senda: Paragraph [0075]).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

AMR A. AWAD
SUPERVISORY PATENT EXAMINER

13 February 2007